DTμL 9111

PARALLEL GATED-CLOCKED FLIP-FLOP

FAIRCHILD DIODE-TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

INDUSTRIAL MICROCIRCUITS - 0°C TO +75°C TEMPERATURE RANGE

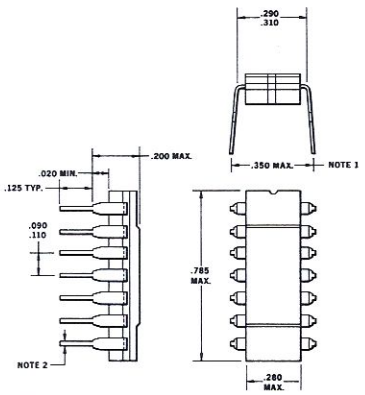
GENERAL DESCRIPTION - The DTμL9111 is a Parallel Gated, Clocked Flip-Flop. It features directly coupled units operating on the "master-slave" principle. Operation is logically and electrically identical to the DTμL9948 with the addition of another pair of two-input gates at the inputs of the flip-flop. This feature enhances the Logic design of some counters and shift-registers and can significantly reduce can count.

A direct clear input is provided which allows asynchronous entry irrespective of signals applied to any other inputs.

Output buffers provide isolation between the "slave" and the output load, thereby enhancing immunity to signal line noise.

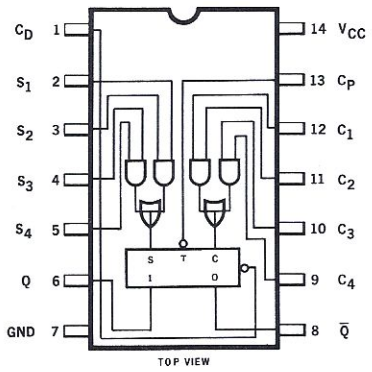
The DTμL9111 is completely compatible with all of the Fairchild 9930 Series Diode-Transistor Micrologic® integrated circuits.

TYPICAL DUAL IN-LINE PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

LOGIC DIAGRAM



TOP VIEW

$f_s = (S_1 \cdot S_2 + S_3 \cdot S_4) C_p$

$f_c = (C_1 \cdot C_2 + C_3 \cdot C_4) C_p + C_D$

INPUT-OUTPUT LOADING FACTORS

(V_{CC} = 5.0 V)

Output Drive

Pins 6 & 8 = 11

Input Loading

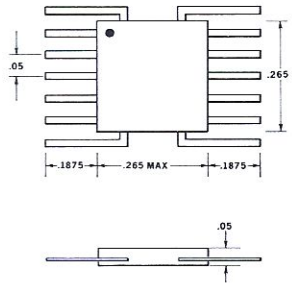
Pins 2, 3, 4, 5, 9, 10, 11, 12 = 2/3

Pin 1 = 2

Pin 13 = 3

TYPICAL FLAT PACKAGE

TOP VIEW



ORDER INFORMATION:

To order the DTμL9111 element, specify the following Part Number:

U31911159X for Flat Pkg.

U6A911159X for Dual In-Line Pkg.

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

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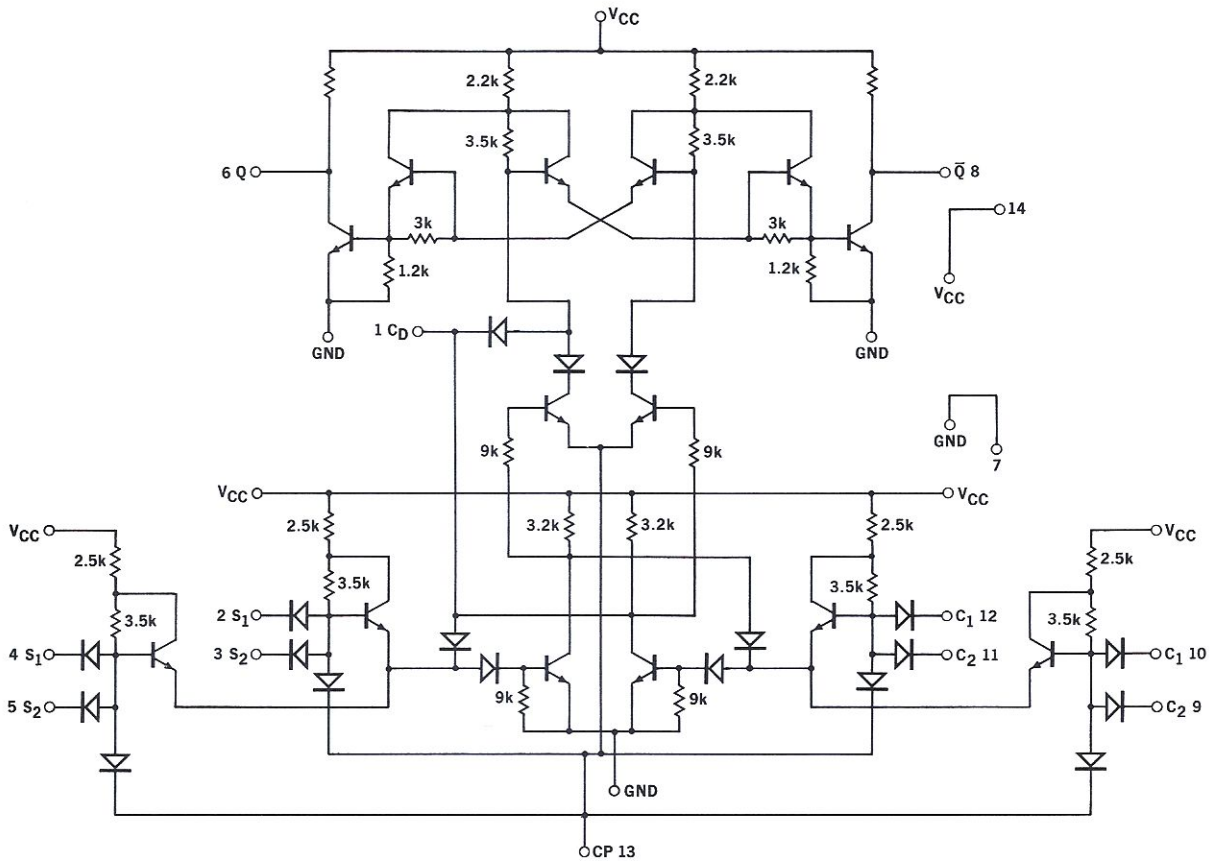
MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U. S. PATENTS: 2981877, 3015048, 3025589, 3064167, 3108359, 3117260; OTHER PATENTS PENDING.

SCHEMATIC DIAGRAM



TRUTH TABLE

SYNCHRONOUS ENTRY

	INPUTS t_n								OUTPUTS t_{n+1}	
Pin	2	3	4	5	9	10	11	12	6	8
	L	X	L	X	L	X	L	X	NC	NC
	X	L	X	L	X	L	X	L	NC	NC
	H	H	X	X	L	X	X	L	H	L
	X	X	H	H	X	L	L	X	H	L
	L	X	X	X	H	H	X	X	L	H
	X	L	L	X	X	X	H	H	L	H
	H	H	X	X	H	H	X	X	Undetermined	
	X	X	H	H	X	X	H	H	Undetermined	

This is a partial table showing significant input-output conditions. Other conditions are similar combinations. Operation is best defined by the set and clear functions shown on Page 1.

For J-K Mode operation:

Connect 6 to 11 and 9; 8 to 3 and 5.

ASYNCHRONOUS ENTRY*

INPUT	OUTPUTS	
Pin 1	6	8
H	NC	NC
L	L	H

*Asynchronous entry is independent of all other inputs and overrides synchronous entry.

NOTES:

(1) Pin numbers refer to flat package or dual in-line package.

(2) Abbreviations used in the body of tables:

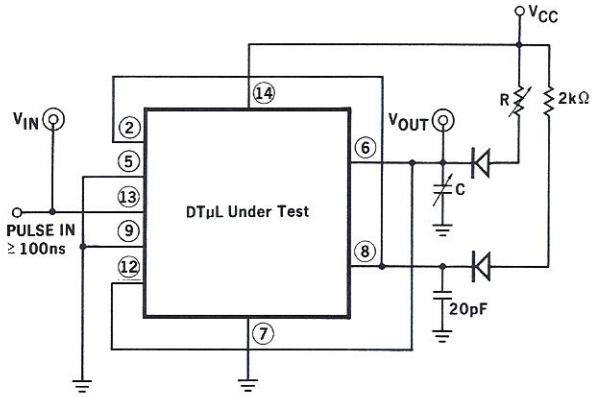
L = low, the more negative voltage level

H = high, the more positive voltage level
(In all cases, unused pins have the same effect as high.)

X = immaterial, either H or L has equal effect

NC = no change, the trigger-pulse has no effect on outputs

tpd TEST CIRCUIT

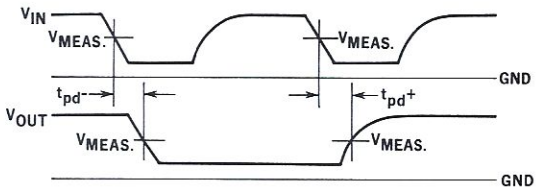


(V_{CC} = 5.0 V, T = 25°C)

	R	C	Min.	Max.
t_{pd+}	2.0 k	30 pF	30 ns	65 ns
t_{pd-}	330 Ω	50 pF	30 ns	75 ns

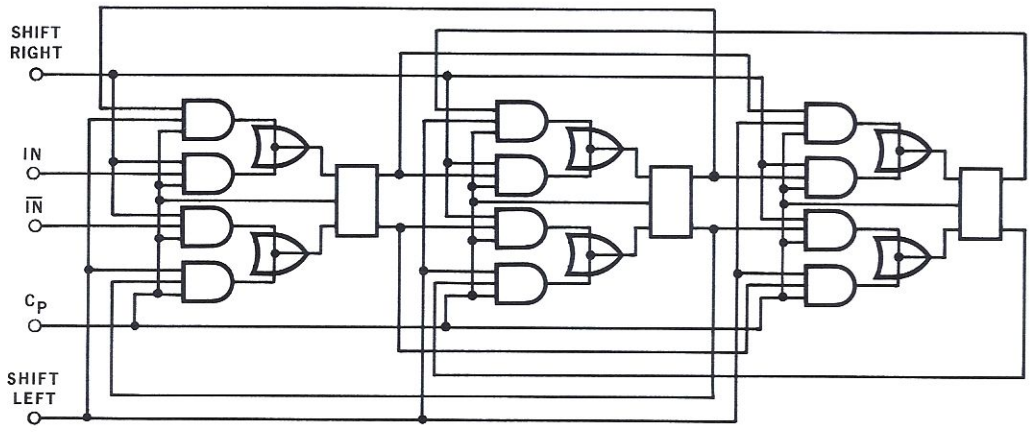
DIODES ARE FD600 OR EQUIVALENT.
ALL C's INCLUDE JIG & PROBE.

WAVE FORMS



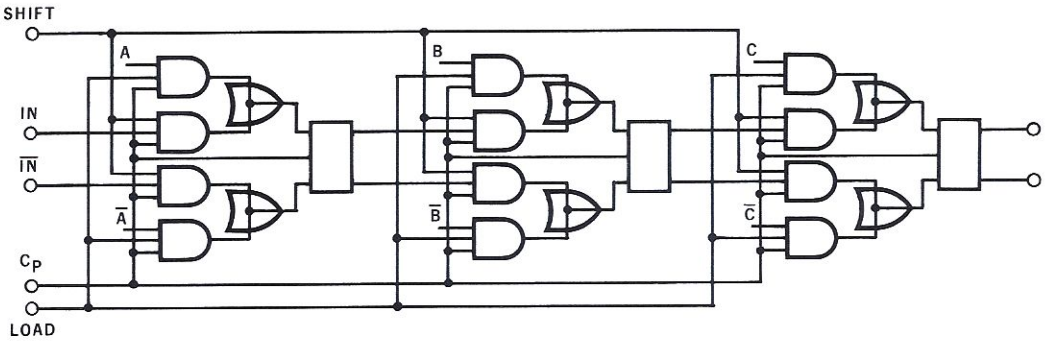
$V_{meas.}$ = 1.5 V at +25°C

TYPICAL APPLICATIONS

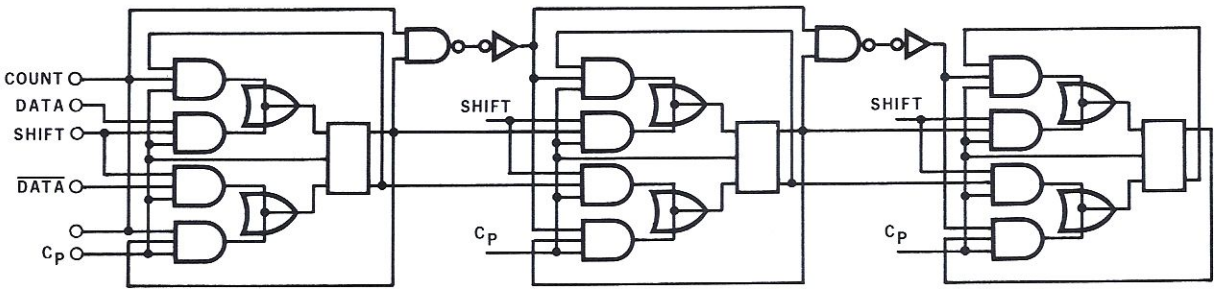


SHIFT RIGHT / SHIFT LEFT SHIFT REGISTER

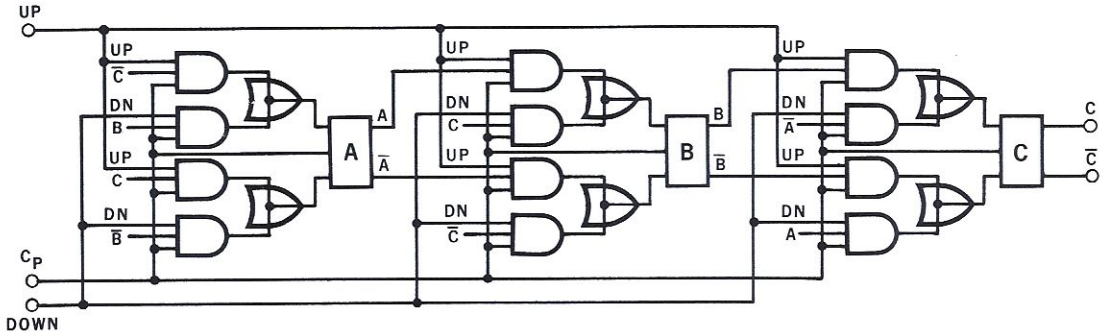
TYPICAL APPLICATIONS



SHIFT REGISTER WITH PARALLEL INPUT LOADING



SERIAL ENTRY - BINARY COUNTER



THREE STAGE MOIBUS COUNTER

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